



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,128	06/27/2003	Ching-Tung Wang	10688-US-PA	1635

31561 7590 08/09/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE  
7 FLOOR-1, NO. 100  
ROOSEVELT ROAD, SECTION 2  
TAIPEI, 100  
TAIWAN

EXAMINER

SHANKAR, VIJAY

ART UNIT PAPER NUMBER

2673

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/604,128

Applicant(s)

WANG ET AL.

Examiner

VIJAY SHANKAR

Art Unit

2673

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 27 June 2003.  
2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-13 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-13 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Priority*

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Morita (US 2002/0190974 A1).

Regarding Claims 1 and 6, Morita teaches a driving circuit for a display (Fig.1; Paragraph 0110-0126), comprising: a timing controller, used to receive a color driving signal, and to output a corresponding color driving signal according to a timing of the timing controller (Paragraph 0070-0091; 0223-0226; 0304-0306); a data controller (Figs.13; Paragraph 0198-0200), having a multi-gray scale, wherein the data controller is coupled to the timing controller to receive the color driving signal, and to make the color driving signal (Paragraph 0070-0091; 0223-0226; 0304-0306) correspond to a related gray of the multi-gray scale according to the multi-gray scale, so as to output a gray-level signal ( Fig.23; Paragraph 0070-0093; 0263-0270) ; and an

inverter (182 in fig.26), coupled to the data controller to receive the gray-level signal and to invert the gray-level signal ( Fig.23; Paragraph 0070-0093; 0263-0270), so as to output a color output signal to the display (fig.23-26; Paragraph 0309-0312, 0321-0326).

Regarding Claim 2, Morita teaches a driving circuit for the display wherein the inverter inverts the gray-level signal according to a voltage level of the gray-level signal. ( Fig.23,26; Paragraph 0076-0083; 0263-0270; 0309-0312).

Regarding Claims 3-4 and 11-12 , Morita teaches the driving circuit for the display wherein the timing controller is further used to receive a clock signal (CLK), a horizontal synchronization signal (HSYNC), a vertical synchronization signal (VSYNC), and a differential enable signal (DE), an ASIC (Application Specific Integrated Circuit) (see paragraph 0118, 0128-0138, 0164-0165).

Regarding Claims 5 and 13, Morita teaches the driving circuit for the display wherein the display is a LCD (Liquid Crystal Display) (10 in fig.1; paragraph 0111).

Regarding Claim 7, Morita teaches the operating method for the display driving circuit wherein the multi-gray scale is included in a data controller in the driving circuit. ( Fig.23; Paragraph 0070-0093; 0263-0270).

Regarding Claim 8, Morita teaches the operating method for the display driving circuit wherein the gray-level signal is inverted by an inverter in the driving circuit. ( Fig.23,26; Paragraph 0076-0083; 0263-0270; 0309-0312).

Regarding Claim 9, Morita teaches the operating method for the display driving circuit wherein the inverter inverts the gray-level signal according to a voltage level of the gray-level signal. ( Fig.23,26; Paragraph 0076-0083; 0263-0270; 0309-0312).

Regarding Claim 10, Morita teaches the operating method for the display driving circuit wherein a timing controller in the driving circuit is used to receive the color driving circuit, and output the color driving circuit according to the timing. (Paragraph 0070-0091; 0223-0226; 0304-0306).

### ***Conclusion***

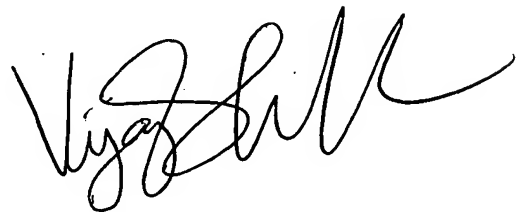
4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Park, and Lee et al teaches the LCD and driving method.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VIJAY SHANKAR whose telephone number is (571) 272-7682. The examiner can normally be reached on M-F 7:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, BIPIN SHALWALA can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



VIJAY SHANKAR  
Primary Examiner  
Art Unit 2673

VS